AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of the claims in this application.

Listing of the Claims:

1. (Previously presented) A system for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a forward fast Fourier transform (FFT) unit calculating a forward fast Fourier transform (FFT) from the data;

a complex multiplication unit receiving the FFT-processed data and calculating a spatial derivative in the frequency domain from the FFT-processed data;

an inverse fast Fourier transform (IFFT) unit converting the spatial derivative in the frequency domain from the complex multiplication unit into the time domain;

a computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from the IFFT unit; and

a memory subsystem that provides input values to the FFT unit and receives output results from the computation engine,

wherein input values for the FFT unit are stored in increasing-x, increasing-y and increasing-z patterns in the memory subsystem that allows a burst read of the memory subsystem to maximize throughput.

2. (Original) A system as recited in claim 1,wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\delta H_{cb}/\delta b + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

3. (Original) A system as recited in claim 1, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

4. (Original) A system as recited in claim 1, wherein the FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

5. (Original) A system as recited in claim 4, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

6. (Previously presented) A system for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a plurality of forward fast Fourier transform (FFT) units, each FFT unit calculating a forward fast Fourier transform (FFT) from the data;

a plurality of complex multiplication units, each complex multiplication unit receiving the FFT-processed data from a corresponding FFT unit and calculating a spatial derivative in the frequency domain from the FFT-processed data;

a plurality of inverse fast Fourier transform (IFFT) units, each IFFT unit converting the spatial derivative in the frequency domain from a corresponding complex multiplication unit into the time domain;

a plurality of computation engines, each computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from a corresponding IFFT unit; and

a memory subsystem that provides input values to the FFT unit and receives output results from the computation engine,

wherein the input values for the FFT unit are stored in increasing-x, increasing-y and increasing-z patterns in the memory subsystem that allows a burst read of the memory subsystem to maximize throughput.

7. (Original) A system as recited in claim 6, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\delta H_{cb}/\delta b + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

8. (Original) A system as recited in claim 6, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

9. (Original) A system as recited in claim 6, wherein the plurality of FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

10. (Original) A system as recited in claim 9, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

11. (Previously presented) A computer hardware configuration for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a forward fast Fourier transform (FFT) unit calculating a forward fast Fourier transform (FFT) from the data;

a complex multiplication unit receiving the FFT-processed data and calculating a spatial derivative in the frequency domain from the FFT-processed data;

an inverse fast Fourier transform (IFFT) unit converting the spatial derivative in the frequency domain from the complex multiplication unit into the time domain;

a computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from the IFFT unit; and

a memory subsystem that provides input values to the FFT unit and receives output results from the computation engine,

wherein the input values for the FFT unit are stored in increasing-x, increasing-y and increasing-z patterns in the memory subsystem that allows a burst read of the memory subsystem to maximize throughput.

12. (Original) A computer hardware configuration as recited in claim 11, wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\delta H_{cb}/\delta b + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

13. (Original) A computer hardware configuration as recited in claim 11, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

14. (Original) A computer hardware configuration as recited in claim 11, wherein the FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

15. (Original) A computer hardware configuration as recited in claim 14, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

16. (Previously presented) A computer hardware configuration for performing the pseudo-spectral time-domain (PSTD) method on data, comprising:

a plurality of forward fast Fourier transform (FFT) units, each FFT unit calculating a forward fast Fourier transform (FFT) from the data;

a plurality of complex multiplication units, each complex multiplication unit receiving the FFT-processed data from a corresponding FFT unit and calculating a spatial derivative in the frequency domain from the FFT-processed data;

a plurality of inverse fast Fourier transform (IFFT) units, each IFFT unit converting the spatial derivative in the frequency domain from a corresponding complex multiplication unit into the time domain;

a plurality of computation engines, each computation engine solving a PSTD equation based upon the spatial derivative in the time domain received from a corresponding IFFT unit; and

a memory subsystem that provides input values to the FFT unit and receives output results from the computation engine,

wherein values for the FFT unit are stored in increasing-x, increasing-y and increasing-z patterns in the memory subsystem that allows a burst read of the memory subsystem to maximize throughput.

17. (Original) A computer hardware configuration as recited in claim 16,wherein the PSTD equation takes the form:

$$E_{ab} = AE_{ab} + B\delta H_{cb}/\delta b + CE_{ab}^{inc},$$

where a, b, and c are directions (x, y, and z), A, B, and C are coefficients based on material properties of a medium, and E_{ab}^{inc} is the incident field associated with the node.

18. (Original) A computer hardware configuration as recited in claim 16, wherein as the FFT is being calculated, primary fields, incident fields, and coefficients are being fetched by the system.

19. (Original) A computer hardware configuration as recited in claim 16, wherein the plurality of FFT and IFFT units are provided inside a field-programmable gate array (FPGA).

20. (Original) A computer hardware configuration as recited in claim 19, wherein the FFT and IFFT calculations are performed by a digital signal processing (DSP) chip.

21- 22. (Canceled).